

APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: PHASE LOCKED LOOP CIRCUIT

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CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV331654788US

February 12, 2004
Date of Deposit

PHASE LOCKED LOOP CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application is based upon and claims the benefit of
priority from prior Japanese Patent Applications No. 2003-
33888, filed on February 12, 2003, and No. 2003-416391, filed
on December 15, 2003, the entire contents of which are
incorporated herein by reference.

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BACKGROUND OF THE INVENTION

 The present invention relates to a phase locked loop
(PLL) circuit that receives a first reference signal, which
15 is generated by superimposing a wobble signal on a land pre-
pit signal, and a second reference signal, which is generated
from a wobble signal, to generate a clock signal synchronized
with either one of the first reference signal and the second
reference signal.

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 Recently, various types of disc-type recording media,
such as optical discs are becoming more popular. Disc
recording media, such as for example, a Digital Versatile
Disc-Recordable (DVD-R), a Digital Versatile Disc-Rewritable
25 (DVD-RW), a Digital Versatile Disc + Recordable (DVD+R), and
a Digital Versatile Disc + ReWritable (DVD+RW) have been
introduced to the market. Although the format of the data
recorded on the disc recording medium is the same in these
disc recording media, the recording format of the disc
30 positional information in DVD-R and DVD-RW media differs from
that in DVD+R and DVD+RW media. The DVD-R and the DVD-RW
(hereinafter referred to as DVD-R/RW) and the DVD+R and the
DVD+RW (hereinafter referred to as DVD+R/RW) are standardized
disc recording media for recording data in compliance with

the same data format, as shown in Fig. 13.

Fig. 13 shows the configuration of one sector of the recording data in a DVD. The DVD data to be recorded on the DVD disc medium consists of 32 bits of synchronizing signal (SYNC in Fig. 13) and 1456 bits of modulated data. In other words, 728 bits of data are 8-16 modulated to produce 1456 bits of data, and 32 bits of a synchronizing signal (SYNC) are added to the head of each of the 1456 bits of modulated data. This generates one frame of recording data. In a DVD, 26 frames of recording data make up one sector.

The recording format of disc positional information recorded on the DVD disc medium differs depending on the type of the DVD disc medium.

The DVD-R/RW is provided with a track formed by a groove, which is formed in a flat surface (land) of the disc. The groove is formed so as to meander at a rate of sixteen cycles for every two frames in a data recording region in the format data (Fig. 14(a)). A wobble signal having a predetermined cycle is extracted from such meandering (wobble) of the groove.

Further, the DVD-R/RW has, in addition to the wobble, a Land Pre-Pit (LPP), which represents disc positional information on the track and which is provided at predetermined intervals. The LPP is provided for every two frames in the data recording region in the above format data. A group of the LPPs that are provided for each of sixteen sectors of the recording region in the above format data represents positional information of the disc.

The DVD+R/RW is also provided with a track formed by a

groove, which is formed in a flat surface (land) of the disc. A wobble signal having a predetermined cycle is extracted from the meandering (wobble) of the groove. The meandering cycle of the DVD+R/RW groove is longer than the meandering cycle of the DVD-R/RW groove. The DVD+R/RW groove meanders at a rate of 93 cycles for every two frames in a data recording region in the above format data.

There are no LPPs formed on the DVD+R/RW. In place of the LPP, the groove is formed so that phase-modulation is performed on the wobble signal of the predetermined cycle in accordance with disc positional information, which is referred to as Address In Pregroove (ADIP). More specifically, the wobble is phase-modulated once for every two frames in the data recording region in the above format data. The ADIPs acquired from each of four sectors of the recording region in the above format data represent the disc positional information.

The recording of data to a disc medium is performed by irradiating a laser beam on the disc medium, the rotation of which is controlled. It is preferred that the recording of data be performed in accordance with a reference clock signal, which corresponds to the rotation of the disc medium. The reference clock signal enables the recording region for every one bit of data that is recorded to the disc medium to be constant and thus enables the recording of data to be accurately controlled.

A PLL circuit uses a reproduced wobble signal or LPP signal to generate a pulse signal, which is synchronized with the wobble signal and the LPP signal, to acquire the reference clock signal. Japanese Laid-Open Patent Publication No. 2002-230915 describes a conventional PLL

circuit. The PLL circuit compares the phase of a clock signal, the oscillation of which is controlled by a voltage-controlled oscillator, and the phase of a wobble signal or LPP signal to calculate a frequency difference between the two signals. Then, the PLL circuit feeds back voltage, which is in accordance with the frequency difference, to the voltage-controlled oscillator. This synchronizes the clock signal with the wobble signal or the LPP signal.

The recording format of the disc position information differs between the DVD-R/RW media and the DVD+R/RW media. Thus, a data recording controller that may be used in a compatible manner for both DVD-R/RW and DVD+R/RW includes a DVD-R/RW clock signal generation circuit and a DVD+R/RW clock signal generation circuit. The circuit scale (size and number of devices) of a clock signal generation circuit is relatively large. This enlarges the circuit scale of a data recording controller provided with both DVD-R/RW and DVD+R/RW clock signal generation circuits.

SUMMARY OF THE INVENTION

One aspect of the present invention is a PLL circuit for receiving either one of first and second reference signals to generate a clock signal synchronized with one of the first and second reference signals. The first reference signal is generated by superimposing a first wobble signal having a first cycle on a land pre-pit signal, and the second reference signal is generated from a second wobble signal having a second cycle shorter than the first cycle. The PLL circuit includes a voltage-controlled oscillator for generating the clock signal in accordance with control voltages. A first loop, connected to the voltage-controlled oscillator, controls at least one of a frequency and a phase

of the clock signal in accordance with one of the first wobble signal and the second wobble signal. A second loop, connected to the voltage-controlled oscillator, controls at least one of the frequency and the phase of the clock signal in accordance with the land pre-pit signal. The first and second loops are validated when the PLL circuit is provided with the first reference signal, and the first loop is validated and the second loop is invalidated when the PLL circuit is provided with the second reference signal.

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A further aspect of the present invention is a PLL circuit for generating a clock signal from a first wobble signal having a first cycle and a land pre-pit signal or from a second wobble signal having a second cycle shorter than the first cycle. The PLL circuit has a voltage-controlled oscillator including a first input terminal and a second input terminal respectively receiving a first control voltage and a second control voltage for generating the clock signal with a frequency and a phase that are in accordance with the first and second control voltages. A first loop, connected to the voltage-controlled oscillator, includes a first divider for dividing the clock signal to generate a first divisional clock signal and a frequency comparator, connected to the first divider, for comparing the frequency of one of the first wobble signal and the second wobble signal with the frequency of the first divisional clock signal. The first loop generates the first control voltage in accordance with the frequency difference between the two compared signals. A second loop, connected to the voltage-controlled oscillator, includes a second divider for dividing the clock signal to generate a second divisional clock signal and a phase comparator, connected to the second divider, for comparing the phase of the land pre-pit signal and the phase of the second divisional clock signal. The second loop generates

the second control voltage in accordance with the phase difference between the two compared signals. The voltage-controlled oscillator is shared by the first and second loops. A voltage generation circuit generates a constant
5 voltage. The first and second input terminals are respectively supplied with the first and second control voltages when the PLL circuit is provided with the first wobble signal and the land pre-pit signal, and the first and second input terminals are respectively supplied with the
10 first control voltage and the constant voltage and the second control voltage is invalidated when the PLL circuit is provided with the second wobble signal.

Other aspects and advantages of the present invention
15 will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

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The invention, together with objects and advantages thereof, may best be understood by reference to the following description of the presently preferred embodiment together with the accompanying drawings in which:

25 Fig. 1 is a block diagram of a PLL circuit according to a preferred embodiment of the present invention;

Fig. 2 is a circuit diagram of a voltage-controlled oscillator shown in Fig. 1;

30 Figs. 3, 4, 5, 6A and 6B are graphs showing the characteristics of the voltage-controlled oscillator of Fig. 2;

Fig. 7 is a timing chart illustrating the waveforms of a wobble signal and an LPP signal;

Fig. 8 is a circuit diagram of a charge pump shown in Fig. 8;

Fig. 9 is a circuit diagram of a rising edge comparator and a charge pump unit shown in Fig. 1;

Fig. 10 is a timing chart illustrating a process for generating a clock signal synchronized with the wobble
5 signal;

Fig. 11 is a circuit diagram of a phase comparator and charge pump unit shown in Fig. 1;

Fig. 12 is a timing chart illustrating a process for generating a clock signal synchronized with the LPP signal;

10 Fig. 13 is a diagram showing the format of the data modulated in a DVD; and

Fig. 14 is a diagram showing the waveforms of a DVD-R wobble signal and a DVD+R wobble signal.

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A PLL circuit incorporated in a data recording controller, adapted to both DVD-R/RW and DVD+R/RW media, according to a preferred embodiment of the present invention
20 will now be discussed.

Fig. 1 is a block diagram of the data recording controller.

25 An optical disc 1 is a disc medium to which data may be written (recorded). In the data recording controller of the preferred embodiment, data may be recorded to both DVD-R/RW and DVD+R/RW media.

30 The data recording controller includes an optical head 10, an RF amp 20, and a clock signal generator 100. The optical head 10 irradiates the optical disc 1 with a laser beam and receives the reflection of the laser beam. The RF amp 20 generates a binary digital signal from the reflection

to generate a wobble signal or an LPP signal.

Based on the wobble signal or the LPP signal, the clock
signal generator 100 functions as a PLL circuit that
5 generates an appropriate clock signal for recording data in
accordance with the type of the optical disc 1 (DVD-R/RW or
DVD+R/RW).

The circuits related to the recording of data when the
10 optical disc 1 is a DVD-R/RW will now be discussed.

The DVD-R/RW includes a spiral pregroove and land
prepits (LPPs), which are arranged between adjacent
pregrooves. The pregroove wobbles and functions as a guide
15 groove for the optical disc 1. A signal having a frequency
of 140.6 kHz is extracted from the wobble of the pregroove.
A signal having a frequency of 140.6 kHz is extracted from
the wobble of the pregroove. The LPPs are formed at
predetermined intervals along the pregrooves. The LPP
20 interval is set to extract a signal having one pulse for
about every sixteen pulses of the wobble signal. The LPPs
are reproduced to extract an LPP signal.

The clock signal generator 100 divides the frequency of
25 the LPP signal by a dividing ratio of 1/2976. In other
words, the clock signal generator 100 generates a clock
signal having 2976 pulses for each pulse interval of the LPP
signal. The frequency of the generated clock signal is 26.16
MHz.

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The clock signal generator 100 synchronizes the
frequency of the recording clock signal with that of the
wobble signal and adjusts the phase of the recording clock
signal based on the LPP signal.

The recording clock signal, which is phase-synchronized to the LPP signal, is generated through two processes in which the recording clock signal is first roughly adjusted based on the wobble signal and then finely adjusted based on the LPP signal. More specifically, after decreasing the frequency difference between the wobble signal and the recording clock signal so that the difference is within a predetermined range, the recording clock signal undergoes phase adjustment based on the LPP signal. This is because it is difficult to generate the recording clock signal directly from the LPP signal since the frequency of the LPP signal is lower than that of the wobble signal and since there may be missing LPPs in the disc medium when recording data.

The clock signal generator 100 includes a first loop L1 and a second loop L2, which share a voltage-controlled oscillator 110. The first loop L1 includes a divider 105, which generates a divisional clock signal by dividing the clock signal output from the voltage-controlled oscillator 110. The first loop L2 synchronizes the frequency of the divisional clock signal of the divider 105 with the frequency of the wobble signal. The second loop L2 includes a divider 176, which generates a divisional clock signal by dividing the clock signal output from the voltage-controlled oscillator 110. The second loop L2 synchronizes the phase of the divisional clock signal with the phase of the LPP signal. The voltage-controlled oscillator 110 includes two control voltage input terminals Ta and Tb. Voltage corresponding to the frequency difference between the divisional clock signal and the wobble signal and voltage corresponding to the phase difference between the divisional clock signal and the LPP signal are respectively applied to the control voltage input terminals Ta and Tb.

The voltage-controlled oscillator 110 will now be described.

Referring to Fig. 2, the voltage-controlled oscillator 110 includes a first current source 112, a second current source 114, a gain control circuit 115, a control voltage generation circuit 116, and a ring oscillator 118.

The first current source 112 performs gain control on the control current corresponding to the control voltage applied to the control voltage input terminal Ta to drive the ring oscillator 118. The first current source 112 has an output current route having a plurality of stages including a plurality of p-channel transistors Tip and a plurality of switches SWi, which are respectively connected in series to the transistors Tip. The p-channel transistors Tip and the switches SWi are connected in parallel to the power supply of the power supply voltage VDD and the output terminal of the first current source 112. The gain control circuit 115 connects and disconnects the power supply and the output terminal in accordance with a control signal, which activates and inactivates each switch SWi, to change the number of stages used in the output current route.

The first current source 112 has an input current route including an n-channel transistor Tan and a p-channel transistor Tap, which are connected in series between the power supply of the power supply voltage VDD and ground. Control voltage is applied to the gate of the n-channel transistor Tan via a control voltage input terminal Ta. The amount of current flowing through the p-channel transistor Tap and the voltage of the gate is determined in accordance with the level of the control voltage. The same voltage as the gate voltage of the p-channel transistor Tap is applied

to the gate of the p-channel transistor Tip, which is a current mirror connected to the p-channel transistor Tap. Further, the same voltage is applied to the gate of the p-channel transistor Tip, which is connected in parallel to the p-channel transistor Tip, to determine the amount of current flowing through the source and drain. Accordingly, the amount of current output from the first current source 112 is controlled in accordance with the level of the control voltage applied to the control voltage input terminal Ta.

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The second current source 114 has the same configuration as the first current source 112. However, the second current source 114 performs gain adjustment on the control voltage input from the control voltage input terminal Tb to drive the ring oscillator 118. The amount of current output from the second current source 114 is controlled in accordance with the level of the control voltage applied to the control voltage input terminal Tb.

The gain control circuit 115 controls the switching between the first current source 112 and the second current source 114 in accordance with mode data stored in a register 115a. That is, the gain control circuit 115 selectively opens and closes switches SWi in the first current source 112 and switches SWk in the second current source 114 to adjust the varying ratio of the output current of the first and second current sources 112 and 114 with respect to changes in the voltage applied to the control voltage input terminals Ta and Tb.

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The control voltage generation circuit 116 converts a current signal, which is output from the first current source 112 and the second current source 114, to a voltage signal. The control voltage generation circuit 116 has a current

mirror circuit, which includes two stages of n-channel transistors T1n and T2n and p-channel transistors T3p and T4p. The gate bias voltage of an n-channel transistor T5n, which is connected in series to the p-channel transistor T4p and the second current mirror circuit, is provided to the ring oscillator 118.

The ring oscillator 118 includes an odd number of inverters IV connected to the power supply of the power supply voltage VDD and the ground. The amount of current provided to each inverter IV is controlled in accordance with the control voltage applied to the control voltage input terminal Ta and the control voltage input terminal Tb. More specifically, a p-channel transistor Tjp is connected between the power supply of the power supply voltage VDD and each inverter IV. A n-channel transistor Tjn is connected between each inverter IV and the ground. Voltage corresponding to the output current of the first current source 112 and the second current source 114 is applied to the transistors Tjp and Tjn via the control voltage generation circuit 116. The transistors Tjp and Tjn control the amount of current that flows to the inverters IV.

The characteristics of the voltage-controlled oscillator 110 will now be described.

Fig. 3 is a graph showing the relationship between the control voltage applied to the control voltage input terminal Ta and the oscillation frequency of the voltage-controlled oscillator 110. Curve f1 is obtained when the voltage applied to the control voltage input terminal Tb is null. Curves f2, f3, and f4 are obtained when the number of output current route stages used in the second current source 114 of Fig. 2 is one, two, and three, respectively. The oscillation

frequency increases as the control voltage applied to the control voltage input terminal Ta increases. When the control voltage applied to the control voltage input terminal Ta is constant, the oscillation frequency increases as the
5 number of stages (number of activated stages) used in the output current route of the second current source 114 increases.

Under the condition that the control voltage applied to
10 the control voltage input terminal Ta is constant, the bandwidth of the oscillation frequency when the voltage applied to the control voltage input terminal Tb is variable, increases as the number of stages used in the output current route of the second current source 114 increases ($\Delta A < \Delta B <$
15 ΔC). Accordingly, when the number of stages used in the output current route of the second current source 114 is fixed to a predetermined number n and the voltage applied to the control voltage input terminal Ta and the control voltage input terminal Tb are variable, the oscillation frequency of
20 the voltage-controlled oscillator 110 is varied within the band indicated by the inclined lines in Fig. 4.

When the voltage applied to the control voltage input terminal Tb is fixed to a null value and the number of stages
25 used in the output current route of the first current source 112 shown in Fig. 2 is changed, the oscillation frequency varies in accordance with the voltage applied to the control voltage input terminal Ta as shown in Fig. 5. The number of stages used in the output current route of the first current
30 source 112 increases from curve f1' to curve f1 to curve f1''. As the number of stages used in the output current route increases, the rate of increase of the oscillation frequency with respect to the change in the voltage applied to the control voltage input terminal Ta increases.

When the roles of the control voltage input terminal Ta and the control voltage input terminal Tb are reversed, the same characteristics as those schematically shown in Figs. 3 to 5 are obtained.

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In the voltage-controlled oscillator 110, which includes the two control voltage input terminals Ta and Tb, the output voltage Va of a low-pass filter 142, which is shown in Fig. 1, is applied to the control voltage input terminal Ta, and the output voltage Vb of a low-pass filter 170, which is shown in Fig. 1, is applied to the control voltage input terminal Tb. This synchronizes the frequency of the clock signal oscillated by the voltage-controlled oscillator 110 (more accurately, the divisional clock signal) with the frequency of the wobble signal through the control voltage input terminal Tb and synchronizes the phase of the clock signal (more accurately, the divisional clock signal) with the phase of the LPP signal through the control voltage input terminal Tb. That is, the control voltage of the control voltage input terminal Ta is used to roughly adjust the oscillation frequency as shown in Fig. 6(b), and the control voltage of the control voltage input terminal Tb is used to finely adjust the oscillation frequency as shown in Fig. 6(b).

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Circuits for performing fine adjustment and rough adjustment of the oscillation frequency of the voltage-controlled oscillator 110 will now be discussed.

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The first loop L1 will first be described.

The first loop L1 compares the rising edges of the recording clock signal, which is oscillated by the voltage-controlled oscillator 110, and the wobble signal. The first

loop L1 also compares the falling edges of the recording clock signal and the wobble signal. Based on the comparison results, the first loop L1 controls the voltage-controlled oscillator 110. The comparisons of the rising edges and the falling edges are performed for the reasons described below.

Referring to Fig. 7(a), the RF amp 20 binary codes and converts the signal corresponding to the wobble of the disc medium read with a laser beam to a wobble signal (Fig. 7(b)). The wobble signal is a signal for which duty ratio changes. Thus, when the voltage-controlled oscillator 110 is controlled based on the phase difference between the divisional clock signal and the wobble signal, the control is affected by the changes in the duty ratio of the wobble signal.

However, referring to Fig. 7(d), the pulse width W_h of the wobble signal changes, but the cycle T_w between the centers of the pulses does not change. Accordingly, the voltage-controlled oscillator 110 is controlled using the cycle T_w and phase of the pulse centers in the wobble signal and the cycle and phase of the pulse centers in the divisional clock signal to avoid the influence of changes in the duty ratio.

More specifically, in the first loop L1 of Fig. 1, a rising edge comparator 120a and a falling edge comparator 120b respectively compares the rising edges and falling edges of the wobble signal and the divisional clock signal. Signals generated from the comparison results are respectively converted to predetermined outputs by a charge pump 130a and a charge pump 130b. The signals of which outputs have been converted are synthesized by an adder 140 and smoothed by a low-pass filter 142 and applied to the

control voltage input terminal Ta of the voltage-controlled oscillator 110 as a control voltage. The frequency of the clock signal, which is oscillated by the voltage-controlled oscillator 110 and controlled by the control voltage, is divided by the divider 105 and input to the rising edge comparator 120a and the falling edge comparator 120b. The clock signal (or its divisional clock signal), which is oscillated from the voltage-controlled oscillator 110, is controlled to be frequency-synchronized with the wobble signal. The dividing ratio of the divider 105 is 1/186 and, in this case, the frequency of the output signal of the voltage-controlled oscillator 110 is 26.16 MHz.

The charge pump 130a, of which gain is variable, is shown in Fig. 8. The charge pump 130a includes a plurality of charge pump units CP, which output current in accordance with the output signal of the rising edge comparator 120a, and a gain switching circuit 131a, which drives selected ones of the charge pump units CP. The gain switching circuit 131a changes the number of stages of the charge pump units CP that are driven to switch the gain of the charge pump 130a, that is, the output current amount level of the charge pump 130a with respect to the phase comparison output.

Referring to Fig. 9, each charge pump unit CP includes an output circuit 132a, which outputs a signal corresponding to the signal received from the rising edge comparator 120a, and a bias circuit 133a, which adjusts the output of the output circuit 132a. When a pulse of the wobble signal rises before the pulse of the divisional clock signal rises, the output circuit 132a outputs a signal having a high potential (performs charging) from when the wobble signal rises to when the divisional clock signal rises. Further, when a pulse of the divisional clock signal rises before the pulse of the

wobble signal rises, the output circuit 132a outputs a signal having a low potential (performs discharging) from when the divisional clock signal rises to when the wobble signal rises.

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In the charge pump 130a, when the charging period is equal to the discharging period, the charge current and the discharge current are set to be equal to each other.

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The rising edge comparator 120a controls the charge pump 130a to generate the predetermined output signal from when the pulse of either one of the input wobble signal and the divisional clock signal rises to when the pulse of the other one of the signals rises. The wobble signal and the

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divisional clock signal are respectively input to different flip-flops (F/F). In synchronism with the rising edge of the input pulse, the flip-flops output a signal having a high level. When the pulses of two flip-flops both rise, the two flip-flops are reset to interrupt the output of the signal

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from the charge pump 130a.

The falling edge comparator 120b and the charge pump 130b of Fig. 1 have the same configuration as the rising edge comparator 120a and the charge pump 130a. As shown in Fig.

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1, the falling edge comparator 120b detects a falling edge when the signal input to the rising edge comparator 120a is inverted by an inverter.

Fig. 10 shows the relationship between the signals input to the rising edge comparator 120a and the falling edge comparator 120b and the output of the adder 140. When the divisional clock signal (Fig. 10(b)) and the wobble signal (Fig. 10(a)) rise and fall at the same timing (β), the output of the adder 140 is substantially null.

In comparison, when the divisional clock signal has a pulse width that is narrower than that of the wobble signal (α in Fig. 10(a)), the adder 140 outputs a signal having a low potential (performs discharging) from when the pulse of the divisional clock signal goes high to when the pulse of the wobble signal goes high, and the adder 140 outputs a signal having a high potential (performs charging) from when the pulse of the divisional clock signal goes low to when the pulse of the wobble signal goes low (refer to α in Fig. 10(c)). The period from when the pulse of the divisional clock signal goes high to when the pulse of the wobble signal goes high is equal to the period from when the pulse of the wobble signal goes low to when the pulse of the divisional clock signal goes low. This equalizes the discharge current and the charge current.

When the pulse width of the divisional clock signal becomes greater than the pulse width of the wobble signal (γ in Fig. 10(a)), the adder 140 outputs a signal having a high potential (performs charging) from when the pulse of the wobble signal goes high to when the pulse of the divisional clock signal goes high, and the adder 140 outputs a signal having a low potential (performs discharging) from when the pulse of the divisional clock signal goes low to when the pulse of the wobble signal goes low (refer to γ in Fig. 10(c)). The period from when the pulse of the wobble signal goes high to when the pulse of the divisional clock signal goes high is equal to the period from when the pulse of the divisional clock signal goes low to when the pulse of the wobble signal goes low. This equalizes the charge current and the discharge current.

In this manner, when the pulse centers are the same, the charge current and the discharge current are equalized with

each other in the charge pumps 130a and 130b. Accordingly, the centers of the wobble signal and the divisional clock signal coincide with each other regardless of the difference between the pulse widths of the wobble signal and the
5 divisional clock signal.

The second loop L2 of Fig. 1 will now be described. The second loop L2 synchronizes the phase of the divisional clock signal of the clock signal oscillated by the voltage-
10 controlled oscillator 110 with the phase of the LPP signal.

In the second loop L2, the period during which the LPP should be detected is predicted in order to distinguish the LPP signal input to the clock signal generator 100 from
15 noise. That is, a command circuit 172 stores the time at which the LPP signal is detected for the first time and, for example, counts the clock signal output from the clock signal generator 100 to predict the period from when the LPP signal is detected to when the next LPP is detected. The command
20 circuit 172 outputs a window pulse at a predetermined cycle in synchronism with the time in which the LPP signal should be detected. The window pulse has a pulse width that covers the period during which there is a possibility that the LPP signal may be detected. In an LPP output circuit 174, the
25 LPP signal is output only when the LPP signal is detected during the period in which the window pulse is input. This avoids erroneous detection of noise as the LPP signal.

A phase comparator 150 compares the phase of the LPP
30 signal output from the LPP output circuit 174 and the phase of the divisional clock signal, which is the clock signal oscillated by the voltage-controlled oscillator 110 divided by the divider 176. A charge pump 160 converts a signal generated from the comparison result to a signal having a

predetermined output level. A low-pass filter 170 then
smoothes the converted signal. The control voltage signal
output from the low-pass filter 170 is applied to the control
voltage input terminal Tb of the voltage-controlled
5 oscillator 110.

The dividing ratio of the divider 176 is determined to
generate the clock signal so that it deviates from the phase
of the LPP signal by a predetermined phase. The phase
10 comparator 150 outputs the signal generated from the
comparison between the LPP signal and the divisional clock
signal only when the LPP signal is output from the LPP output
circuit 174. Thus, the phase comparator 150 compares the
divisional clock signal, which is generated by dividing the
15 clock signal oscillated from the voltage-controlled
oscillator 110 by a dividing ratio of $1/2976$, and the LPP
signal to adjust the frequency of the clock signal oscillated
from the voltage-controlled oscillator 110 by 26.12 MHz.

20 The comparison of the LPP signal and the divisional
clock signal is controlled so that the rising edge of the
pulses input to the phase comparator 150 from the voltage-
controlled oscillator 110 via the divider 176 coincides with
the pulse centers of the LPP signal input to the phase
25 comparator 150. Fig. 11 shows an example of the
configuration of the LPP output circuit 174 and the phase
comparator 150 that perform such control. As shown in Fig.
11, the charge pump unit CP, which is connected to the output
side of the phase comparator 150, is incorporated in the
30 charge pump 160. The charge pump 160 has the same
configuration as the charge pump 130a of Fig. 8.

Fig. 12 shows the relationship between the window pulse
and LPP signal, which are shown in Fig. 1, the divisional

clock signal, which is output from the divider 176, and the output of the charge pump 160.

Even if noise is mixed (Fig. 12(b)) in with the LPP
5 signal during the period in which the window pulse is not
input to the LPP output circuit 174, such a signal is not
output to the phase comparator 150. Conversely, if the LPP
signal is input (Fig. 12(b)) when the window pulse (Fig.
12(a)) is input to the LPP output circuit 174, the LPP signal
10 is output to the phase comparator 150. This outputs a signal
having a high potential during the period from when the LPP
signal is input to the phase comparator 150 to when the pulse
of the divisional clock signal (Fig. 12(c)) goes high.
During the period in which the pulse of the LPP signal is
15 input and the pulse of the divisional clock signal goes high
(Fig. 12(c)), the charge pump 160 outputs a signal at a high
potential.

The charge pump 160 is set so that the charge current
20 and the discharge current are equalized when the charging
time is equal to the discharging time. As a result, the
charging time and the discharging time are equalized when the
rising edge of the divisional clock signal coincides with the
center of the LPP signal. This equalizes the charge current
25 and the discharge current. In this manner, the voltage-
controlled oscillator 110 is controlled based on the output
signal of the charge pump 160 so that the rising edge of the
pulse of the divisional clock signal output from the divider
176 coincides with the pulse of the LPP signal.

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The fine adjustment with the second loop L2 synchronizes
the frequencies of the clock signal, which is oscillated by
the voltage-controlled oscillator 110, and the wobble signal
while synchronizing the phases of the clock signal and the

LPP signal. Thus, even if the LPP signal of Fig. 7(c) and the center of the wobble signal fluctuates as shown in Fig. 7(d), the clock signal oscillated from the voltage-controlled oscillator 110 is controlled to be phase-synchronized with
5 the LPP signal.

The two-step process using the first loop L1 and the second loop L2, that is, the rough adjustment for synchronizing the frequencies of the clock signal and the
10 wobble signal, and the fine adjustment for synchronizing the phases of the clock signal and the LPP signal will now be discussed. A first monitor circuit 180, a second monitor circuit 182, and a control circuit 186 perform the rough adjustment and fine adjustment.

15

The first monitor circuit 180 receives the wobble signal and the divisional clock signal of the divider 105 to monitor whether the first loop L1 has completed frequency
20 synchronization of the wobble signal and the divisional clock signal.

The second monitor circuit 182 receives the LPP signal and the divisional clock signal of the divider 176 to monitor the conditions of the LPP signal and the divisional clock
25 signal processed by the second loop L2.

The control circuit 186 controls the first monitor circuit 180 and the second monitor circuit 182 to perform the rough adjustment and the fine adjustment in accordance with
30 the signals from the first monitor circuit 180 and the second monitor circuit 182.

In a data recording controller having such a configuration, circuits for performing data recording when

the optical disc 1 is a DVD+R/RW will now be described.

A DVD+R/RW includes a pregroove, which functions as a guide groove for the disc. The pregroove wobbles along the optical disc 1. A signal having a wobble component has a frequency of 817.5 kHz. The clock signal generator 100 generates a clock signal by dividing the frequency of the wobble signal by a dividing ratio of 1/32.

When the optical disc 1 is a DVD+R/RW, the first loop L1 synchronizes the clock signal output from the voltage-controlled oscillator 110 with the wobble signal of the DVD+R/RW. More specifically, the dividing ratio of the divider 105 is set to 1/32 to control the frequency of the clock signal, which is oscillated by the voltage-controlled oscillator 110 based on the 817.5 kHz wobble signal, to control the frequency of the clock signal oscillated by the voltage-controlled oscillator 110 at 26.16 MHz. In such a state, the second loop L2 is controlled as an open loop, and a constant voltage is applied to the control voltage input terminal Tb of the voltage-controlled oscillator 110.

To perform such controlling, the preferred embodiment includes a voltage generation circuit 184, which outputs a constant voltage to the low-pass filter 170 of the second loop L2, and a switching circuit 185, which connects and disconnects the voltage generation circuit 184 and the low-pass filter 170. The voltage generation circuit 184 generates a predetermined DC voltage. Further, the switching circuit 185 is controlled by a control circuit 186.

The control for generating the clock signal with the clock signal generator 100 when the optical disc 1 is a DVD+R/RW and when the optical disc 1 is a DVD+R/RW will now be

described.

An external circuit outside the clock signal generator 100, such as a microcomputer for centrally controlling each circuit of the data recording controller, inputs to the control circuit 186 a mode signal indicating the type of the optical disc 1 (DVD-R/RW or DVD+R/RW). Further, the external circuit writes mode data to the register 115a in the gain control circuit 115 of the voltage-controlled oscillator 110 shown in Fig. 2. Based on the mode data, the voltage-controlled oscillator 110 sets the number of stages used in the output current route of the first current source 112 and the second current source 114 so that the gain (drive capacity) is in accordance with the type of the optical disc 1.

In the control circuit 186 of Fig. 1, the charge pumps 130a and 130b set the drive capacity that is set in accordance with the optical disc 1. The setting of the drive capacity of the charge pumps 130a and 130b with the control circuit 186 is performed by outputting a command signal to the gain switching circuit of Fig. 8 or a corresponding circuit.

Further, the control circuit 186 switches the switching circuit 185 to apply the voltage output from the voltage generation circuit 184 to a low-pass filter 170 while inactivating a charge pump 160. That is, in a charge pump 160 having the same configuration as that of Fig. 8, an enable signal is not applied to any of the charge pump units CP so that every one of the charge pump units CP are inactivated.

This series of processes end the initialization of the

clock signal generator 100. The generation of the recording clock signal subsequent to the initialization will now be described for when the optical disc 1 is a DVD-R/RW and when the optical disc 1 is a DVD+R/RW.

5

[Example in which the optical disc 1 is a DVD-R/RW]

When the clock signal generator 100 receives the wobble signal, the first loop L1 synchronizes the frequencies of the clock signal oscillated by the voltage-controlled oscillator 110 (actually, the divisional clock signal divided by the divider 105) and the wobble signal. In this state, the second loop L2 inactivates the charge pump 160, and the DC current voltage of the voltage generation circuit 184, or constant voltage, is applied to the control voltage input terminal Tb of the voltage-controlled oscillator 110. At this point in time, the second loop L2 is controlled as an open loop and invalidated.

In the first loop L1, when the first monitor circuit 180 detects that the difference between the frequencies of the divisional clock signal of the clock signal oscillated by the voltage-controlled oscillator 110 and the wobble signal is included within a predetermined range, the control circuit 186 switches the second loop L2 to a closed loop. That is, the switching circuit 185 is switched so that a predetermined number of charge pump units CP in the charge pump 160 are driven and so that the voltage of the voltage generation circuit 184 is not applied to the low-pass filter 170. This applies voltage to the control voltage input terminal Tb of the voltage-controlled oscillator 110 in correspondence with the difference between the phases of the clock signal oscillated by the voltage-controlled oscillator 110 (actually, the divisional clock signal generated by the

divider 176) and the LPP signal.

In addition to the switching, the control circuit 186 performs control to lower the drive capacity of the charge
5 pumps 130a and 130b. This lowers the significance of the first loop L1 in comparison with that of the second loop L2 after the difference between the frequencies of the wobble signal and the recording clock signal decreases. That is, after the synchronization of the wobble signal and the
10 recording clock signal is substantially completed, the recording clock signal is subtly affected by the first loop L1. Thus, the control enables fine adjustment of the recording clock signal with the second loop L2.

15 Further, when rough adjustment is being performed by the first loop L1, the voltage of the voltage generation circuit 184 is applied to the control voltage input terminal Tb of the voltage-controlled oscillator 110 to smooth switching by fine adjustment with the second loop L2. This prevents the
20 oscillation frequency from suddenly changing due to a sudden fluctuation in the value of the voltage applied to the control voltage input terminal Tb when switching the charge pump 160 from an inactivated state to an activated state.

25 It is preferred that the voltage applied to the control voltage input terminal Tb based on the voltage generation circuit 184 be set to be about the same as the voltage assumed to be applied to the control voltage input terminal Tb by the second loop L2 when the phases of the clock signal
30 oscillated by the voltage-controlled oscillator 110 and the LPP signal are synchronized. This minimizes fluctuation of the value of the voltage applied to the control voltage input terminal Tb of the voltage-controlled oscillator 110 when the charge pump 160 is switched from an inactive state to an

active state.

Further, it is preferred that the voltage applied to the control voltage input terminal Tb based on the voltage generation circuit 184 be a substantially median value
5 between the maximum and minimum values of the voltage applied to the control voltage input terminal Tb.

[Example in which the optical disc 1 is a DVD+R/RW]

10

When the clock signal generator 100 receives the wobble signal, the first loop L1 synchronizes the frequencies of the clock signal oscillated by the voltage-controlled oscillator 110 (actually, the divisional clock signal divided by the
15 divider 105) and the wobble signal. In the second loop L2, the charge pump 160 is inactive and the DC voltage of the voltage generation circuit 184, or constant voltage, is applied as the control voltage to the control voltage input terminal Tb of the voltage-controlled oscillator 110. When
20 the optical disc 1 is a DVD+R/RW, the second loop L2 is controlled as an open loop.

When the optical disc 1 is a DVD+R/RW, the gain of the first loop L1 differs from when the optical disc 1 is a DVD-
25 R/RW. That is, due to the difference in the frequencies of the wobble signals, appropriate controlling with different gains is enabled. For example, since the wobble signal of the DVD-R/RW is lower than the frequency of the wobble signal of the DVD+R/RW, it is preferred that the gain, until the
30 frequency difference of the first loop L1 is included in the predetermined range for the DVD-R/RW, be greater than that of the DVD+R/RW.

The gain adjustment is performed by adjusting the gain

(drive capacity) of the voltage-controlled oscillator 110 or the charge pumps 130a and 130b.

Further, the voltage generation circuit 184 may generate
5 different voltages. This enables appropriate controlling in accordance with whether the optical disc 1 is a DVD-R/RW or a DVD+R/RW.

The preferred embodiment has the advantages described
10 below.

(1) When the optical disc 1 is a DVD-R/RW, the recording clock signal is generated with the first loop L1 and the second loop L2. When the optical disc 1 is a DVD+R/RW, the
15 recording clock signal is generated with the first loop L1. This generates an operation clock signal that is in accordance with the type of the optical disc 1.

(2) When the optical disc 1 is a DVD+R/RW, constant
20 voltage is applied to the control voltage input terminal Tb of the voltage-controlled oscillator 110. Thus, the clock signal generator used when the optical disc 1 is a DVD-R/RW is also used to appropriately generate a clock signal when the optical disc 1 is a DVD+R/RW. In addition, by adjusting
25 the voltage applied to the control voltage input terminal Tb of the voltage-controlled oscillator 110, the control parameter for generating the clock signal when the optical disc 1 is a DVD+R/RW is increased. This increases freedom for generating the clock signal.

30

(3) The drive capacity of the voltage-controlled oscillator 110 and the drive capacity of the charge pump 130a differs when the optical disc 1 is a DVD-R/RW and when the optical disc 1 is a DVD+R/RW. Thus, when there is a

difference between the frequencies of the wobble signals, feedback control is properly performed when the clock signal is generated.

5 (4) The dividing ratios of the divider 105 and the divider 176 differ when the optical disc 1 is a DVD-R/RW and when the optical disc 1 is a DVD+R/RW. More specifically, the dividing ratios of the divider 105 and the divider 176 when the optical disc 1 is a DVD-R/RW is smaller than when
10 the optical disc 1 is a DVD+R/RW. This generates the recording clock signal properly from each wobble signal.

 (5) The first loop L1 and the second loop L2 share the voltage-controlled oscillator 110. This reduces the circuit
15 scale of the clock signal generator 100.

 (6) The voltage-controlled oscillator 110 incorporates the first current source 112 and the second current source 114. This enables the characteristics of the voltage-
20 controlled oscillator 110 to be variable.

 (7) The gains of the charge pumps 130a and 130b in the first loop L1 are variable. The gain is decreased when switching from rough adjustment to fine adjustment. This
25 enables the second loop L2 to perform fine adjustment in an optimal manner.

 (8) The command circuit 172 predicts the period during which the LPP signal is detected and enables the phase
30 comparator 150 to perform processing only during the predicted period. This prevents noise from being erroneously recognized as the LPP signal.

 (9) The rising edges and the falling edges of the pulses

of the divisional clock signal, which is generated from the clock signal oscillated by the voltage-controlled oscillator 110, and the wobble signal are compared to control the voltage-controlled oscillator 110 while eliminating the
5 influence of changes in the duty ratio of the reproduced wobble signal.

It should be apparent to those skilled in the art that the present invention may be embodied in many other specific
10 forms without departing from the spirit or scope of the invention. Particularly, it should be understood that the present invention may be embodied in the following forms.

The signal input to the first loop L1 does not have to
15 be a wobble signal and may be a divisional signal of the wobble signal.

The signal input to the second loop L2 is not limited to the LPP signal and may be a divisional signal of the LPP
20 signal.

The configuration of the voltage-controlled oscillator 110 is not limited to that shown in Fig. 2. For example, the current control devices that control the amount of power
25 supplied to each inverter IV of the ring oscillator 118 does not have to be configured by an n-channel transistor and a p-channel transistor.

The gain of the voltage-controlled oscillator 110 is
30 used to initialize the register 115a. However, the gain may be variable when the clock signal generator is operating. Such a configuration is especially effective when the clock signal generator is applied to a data recording device in which the angular velocity is constant.

The configurations of the rising edge comparator 120a, the falling edge comparator 120b, the phase comparator 150, and the charge pumps 130a, 130b, and 160 are not limited to the configurations shown in Figs. 8, 9, and 11.

5

The comparison of the wobble signal and the clock signal, which is oscillated by the voltage-controlled oscillator 110, in the first loop that generates the clock signal, which is the frequency synchronized with the wobble signal, does not have to be performed with both the rising edges and the falling edges. For example, only the rising edge may be used to generate a signal that is substantially synchronized with the wobble signal.

15 The process for generating the window pulse in the command circuit 172 of Fig. 1 may be eliminated, for example, when noise is erroneously detected as the LPP signal.

20 The present invention is not limited to a configuration in which a first loop L1 and a second loop L2 share a voltage-controlled oscillator. In other words, the first loop L1 and the second loop L1 may each incorporate a different voltage-controlled oscillator. In such a case, the voltage applied to the control voltage input terminal of the second loop K2 is switched in the same manner as in the preferred embodiment to minimize fluctuation of the oscillation frequency of the voltage-controlled oscillator when the second loop L2 is switched from opened loop control to closed loop control.

30

The dividing ratios of the dividers 105 and 176 are not limited to those ratios of the preferred embodiment. For example, even if there is a demand for 186 pulses in each cycle of a wobble for the clock signal that actually controls

data recording, the dividing ratio may be set to 372. Such setting enables various demands to be met appropriately during the recording of data.

- 5 The configuration of the data recording controller is not limited to that shown in Fig. 1.

10 The present examples and embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalence of the appended claims.